REMARKS

The Office Action dated July 1, 2005, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 1-6, 8-12, and 15 have been amended. Applicants submit that the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, Claims 1-15 are pending in the present application and are respectfully submitted for consideration.

Specification

The disclosure was objected to as containing some informalities. This objection is respectfully traversed.

In making the objection, the Office Action asserts that

> the disclosure [0015] is not clear because according to figure 1 of the present application, when the input voltage is lower than a threshold value, the voltage across resistor R2 is low. If transistor Q2 is turned on, transistor Q6 is also turned on because its base is also connected to a same low voltage. If the input voltage is higher than a threshold value, the bases of PNP transistors Q1 and Q2 are both high and both transistors are turned off, not turned on as disclosed and the output (3) is indeterminate.

With respect to the Office Action's position regarding the disclosure that "when the input voltage is lower than the threshold value, if the transistor Q2 is on, then the transistor Q6 is on," Applicants respectfully submit that when the input voltage is lower than the threshold value, the transistor Q1 is on, the transistor Q2 is off. In this state, since the transistor Q2 is off, no current flows at the bases of the transistors Q4 and Q5,

which together form a current mirror circuit. Thus, no current flows through this current mirror circuit. Consequently, a current flows at the base of transistor Q6, and thus the transistor Q6 is on.

As for the Office Action's assertion that "when the input voltage is higher than the threshold value, the transistors Q1 and Q2 are both off." Applicants respectfully submit that when the input voltage (i.e., the voltage applied to the input terminal 1) is lower than the threshold value Vs, and since the potential difference between both ends of the resistor R2 is small, Vq1 > Vq2.

According to one embodiment of the present invention, Vq1 represents the base voltage of the transistor Q1, and Vq2 represents the base voltage of the transistor Q2. In this state, since the base voltage Vq2 of the transistor Q2 is low, only the transistor Q1 is on, and transistor Q2 is not on.

Also, when the input voltage (i.e., the voltage applied to the input terminal 1) is higher than the threshold value Vs according to one example of the invention, the potential difference between both ends of the resistor R2 is large. In this state, since the input voltage (i.e., the voltage applied to the input terminal 1) is also high, Vq1 < Vq2. Further in this state, not only the base voltage Vq2 of the transistor Q2 but also the base voltage Vq1 of the transistor Q1 is high, and thus the transistors Q1 and Q2 are both on.

Hence, it is submitted that the disclosure of the application is in compliance with US patent practice, and therefore no correction is necessary.

35 U.S.C. § 112, 2nd Paragraph

Claims 1-12 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. This rejection is respectfully traversed.

Regarding claims 1 and 7, the Office Action interprets the input voltage as Vs and the threshold value as Vf1, and asserts that the recitation "wherein whether the input voltage is equal to a predetermined level or not is checked based on an output from the differential pair" is indefinite.

However, Applicants submit that Fig. 1 illustrates an example where the input voltage (i.e., the voltage applied to the input voltage 1) is equal to the threshold value Vs, and therefore the threshold value is NOT Vf1 but rather Vs. Thus, Fig. 1 illustrates one example of a circuit that checks whether or not the value of the voltage (without sign) applied to the input terminal 1 is equal to the threshold value Vs.

Regarding claim 3, the Office Action asserts that, since "the serial circuit (Q3)" is connected at one end of the first resistor (R1), the recitation "another end of the serial circuit is connected at one end of the second resistor . . . " is indefinite.

Applicants respectfully submit that claim 3 of the present application recites, in part, a serial circuit composed of a rectifying element (e.g., Q3) and a first resistor (e.g., R1), and does NOT recite that "the serial circuit (Q3)" is connected to one end of the first resistor (R1) as the Office Action mistakenly asserted. Thus, Applicants request reconsideration based the above clarification of the claims.

Also regarding claims 3 and 5, these claims along with other claims, have been amended to obviate the rejection.

Regarding claims 5, 11 and 15, it is submitted that claims 1, 5, 11 and 15 have been amended to obviate this rejection.

As for the rejection of "claim 17," the Office Action asserts that the recitation "the serial circuit" is indefinite.

Applicants submit that there is no such claim 17. Assuming arguendo that the remarks noted in the Office Action is actually direct to claim 3 of the present application, then it is submitted that claim 3 recites "a serial circuit composed of a rectifying element and a first resistor" is recited prior to "the serial circuit". Thus, "the serial circuit" in claim 3 is definite and in compliance with US patent practice.

In view of the above, Applicants respectfully submit reconsideration of claims 1-15 of the present application.

Claims 1, 6, 7, 9, 10 and 12-14 Rejected under 35 U.S.C. § 102

Claims 1, 6, 7, 9, 10 and 12-14 were rejected under 35 U.S.C. § 102 as being anticipated by the Admitted Prior Art (hereinafter "APA"). This rejection is respectfully traversed.

Claim 1 recites a voltage detection circuit comprising, among other features, a voltage division circuit that divides an input voltage into a first division voltage and a second division voltage, the voltage division circuit being connected directly to a base of the first transistor to apply the first division voltage to the base of the first transistor, the voltage division circuit being connected directly to a base of the second transistor to apply the second division voltage to the base of the second transistor, and a fourth

resistor that has one end thereof connected to the base of the second transistor and that has another end thereof connected to the emitter of the second transistor.

Claim 7 recites a semiconductor integrated circuit device comprising, among other features, a voltage division circuit that divides an input voltage into a first division voltage and a second division voltage, the voltage division circuit being connected directly to a base of the first transistor to apply the first division voltage to the base of the first transistor, the voltage division circuit being connected directly to a base of the second transistor to apply the second division voltage to the base of the second transistor; and a resistor that has one end thereof connected to the base of the second transistor and that has another end thereof connected to the emitter of the second transistor.

Claim 13 recites a method for fabricating a semiconductor integrated circuit device comprising, among other features, a voltage division circuit including a serial circuit composed of a rectifying element and a first resistor, a second resistor, and a third resistor, the voltage division circuit dividing an input voltage into a first division voltage and a second division voltage, the voltage division circuit being connected directly to a base of the first transistor to apply the first division voltage to the base of the first transistor, the voltage division circuit being connected directly to a base of the second transistor to apply the second division voltage to the base of the second transistor; and a resistor that has one end thereof connected to the base of the second transistor and that has another end thereof connected to the emitter of the second transistor.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicants' invention.

For example, APA merely discloses,

> [a] voltage detection circuit shown in Fig. 4, [where] the voltage division factor of the voltage division circuit composed of the resistors r1 to r3 and the diode-connected transistor Tr1, the base-emitter voltage of the transistor Tr4, the base-emitter voltage of the transistor Tr5, the resistance of the resistor r4, and the resistance of the resistor r5 are so set that the temperature coefficient of the predetermined level V_{sh} is equal to zero. This means that the voltage detection circuit shown in Fig. 4 is absolutely required to be provided with the resistors r1 to r3, the transistor Tr1, the transistor Tr4, the transistor Tr5, the resistor r4, and the resistor r5.
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> As a result, the voltage detection circuit shown in Fig. 4, in which the temperature coefficient of the predetermined level V_{sh} used as the reference level for voltage detection can be made equal to zero, requires a larger number of circuit elements than a voltage detection circuit in which the reference level for voltage detection varies with temperature. Since an increase in the number of circuit elements constituting a circuit hampers its cost reduction and miniaturization, it is desirable to minimize such an increase in the number of circuit elements used. However, the voltage detection circuit shown in Fig. 4 is not composed of the minimum needed number of circuit elements.

As provided above, the voltage division circuit provided in the voltage detection circuit as shown in Fig. 4 of the subject application is composed NOT of resistors r1 to r4 and a transistor Tr1, but rather of transistors r1 to f3 and a transistor Tr1. Thus, in the voltage detection circuit as shown in Fig. 4 of the subject application, a resistor r4 is provided between the voltage division circuit and the second transistor (Tr4), and

therefore the voltage detection circuit is not directly connected to the base of the second transistor (Tr4).

Thus, Applicants submit that the cited prior art fails to disclose or suggest each and every element recited in claims 1, 7 and 13 of the present invention, and therefore is not anticipated by the APA.

Moreover, to qualify as prior art under 35 U.S.C. §102, a single prior art reference must teach, i.e., identically describe, each feature of a rejected claim. As explained above, APA fails to disclose or suggest each and every feature of claims 1, 7 and 13. Accordingly, Applicants respectfully submit that claims 1, 7 and 13 are not anticipated by nor rendered obvious by the disclosure of APA. Therefore, Applicants respectfully submit that claims 1, 7 and 13 are allowable.

As claim 6 depends from claim 1, claims 9, 10 and 12 depend from claim 7, and claim 14 depends from claim 13, Applicants submit that each of these claims incorporates the patentable aspects therein, and are therefore allowable for at least the reasons set forth above with respect to the independent claims, as well as for the additional subject matter recited therein.

Accordingly, Applicants respectfully request withdrawal of the rejection.

Claims 2-4 and 8 Rejected under 35 U.S.C. § 103(a)

Claims 2-4 and 8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the APA. This rejection is respectfully traversed.

As claims 2-4 depend from claim 1, and claim 8 depends from claim 7, Applicants submit that each of these claims incorporates the patentable aspects therein,

and are therefore allowable for at least the reasons set forth above with respect to the independent claims, as well as for the additional subject matter recited therein.

Accordingly, Applicants respectfully request withdrawal of the rejection.

Conclusion

In view of the above, Applicants respectfully submit that each of claims 1-15 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 1-15 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicant respectfully petitions for an appropriate extension of time.

Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, referring to client-matter number 103213-00076.

Respectfully submitted,

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